REMARKS/ARGUMENTS

In response to the outstanding office action, the pending claims have been cancelled and 9 new claims have been added, both in an effort to reduce the number of claims, and to better focus on the aspect of the invention sought to be patented in this application.

The new claims focus on the aspect of the invention of using a one bit sigma delta converters to provide single bit data streams between an analog integrated circuit and a digital integrated circuit without a data rate clock signal also being provided between the analog and the digital integrated circuits. This is contrary to the prior art, but is advantageous to avoid the interference that coupling a data rate clock signal between integrated circuits would generate. In that regard, Maligeorgos recognizes interference problems in general (see col. 11, lines 55-65), but addresses the problems by partitioning the circuits between integrated circuits. Maligeorgos still couples a data clock between circuits, as is common in the prior art.

> "The receiver digital circuitry 905 communicates with the baseband processor circuitry 120 through a set of serial interface signal lines 920. The serial interface signal lines 920 preferably include a serial data-in (SDI) signal line 925, a serial clock (SCLK) signal line 930, a serial interface enable (SENB) signal line 935, and a serial data-out (SDO) signal line 940." (Maligeorgos, col. 22, lines 11-17)

Obviously the serial clock is the serial data clock, as the phrase serial clock is otherwise meaningless. This technique, while creating noise, is manageable for lower frequency sampling rates, as are used for GSM, but in systems that would require a high frequency sampling rate, it would be particularly difficult to use a single bit sigma delta converter, such as in wideband CDMA, while coupling a data clock between analog and digital integrated circuits. The present invention eliminates the interference that would occur by coupling a data rate clock signal between the analog integrated circuit and the digital integrated circuit by not coupling the data rate clock, but by reconstructing the data rate clock on the digital integrated circuit. This allows clear separation of the analog and digital functions, allowing use of a conventional DSP for the digital functions in high sampling clock sigma delta radio systems. Clearly this is not shown in, or obvious from, Maligeorgos or the other prior art cited by the examiner, either alone or in combination. Accordingly it is believed that the new claims are allowable over the prior art.

CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/14/2007

By _____
Roger W. Blakely, Jr.
Reg. No. 25,831
Tel.: (714) 557-3800 (Pacific Coast)

1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☒ *deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.*

Date: 11/14/2007

FACSIMILE

☐ *transmitted by facsimile to the Patent and Trademark Office.*

Jessica A. Clark 11/14/2007

Jessica A. Clark *Date*